FMC-500M

V 1.3 12/8/2016

FMC Module with Dual 500 MSPS 14-bit A/D, Dual 1200 MSPS 16-bit DAC with PLL and Timing Controls (Preliminary)

FEATURES

- Two A/D Inputs
  - 500 MSPS, 14-bit
  - AC or DC coupled
- Two D/A Outputs
  - 1200 MSPS, 16-bit D/A
  - AC or DC coupled
- Sample clocks and timing and controls
  - External clock/reference input
  - Programmable PLL
  - 100 MHz, 0.5 ppm reference
  - Integrated with FMC triggers
- FMC module, VITA 57.1
  - High Pin Count no SERDES required
  - Compatible with 2.5V VADJ
  - Power monitor and controls
- 12 W typical
- Conduction Cooling per VITA 20 subset
- Environmental ratings for -40 to 85C
  9g RMS sine, 0.1g2/Hz random vibration

APPLICATIONS

- Wireless Receiver and Transmitter
- LTE, WiMAX Physical Layer
- RADAR
- Medical Imaging
- High Speed Data Recording and Playback

SOFTWARE

- MATLAB/VHDL FrameWork Logic

DESCRIPTION

The FMC-500M is a high speed digitizing and signal generation FMC IO module featuring two 500MSPS A/D channels and two 1200 MSPS D/A channels supported by sample clock and triggering features.

The FMC-500M features a dual channel, 14-bit 500MSPS A/D device plus a dual 1200 MSPS update rate DAC device. Analog IO may be either AC or DC coupled. Receiver IF frequencies of up to 500 MHz are supported due to the wide bandwidth analog front-end. The sample clock may be sourced from either a low-jitter PLL or external input. Multiple cards can be synchronized for sampling to address MIMO applications.

The FMC-500M power consumption is 12 W for typical operation. The module may be conduction cooled using VITA20 standard and a heat spreading plate. Ruggedization levels for wide-temperature operation from -40 to +85C operation and 0.1 g^2/Hz vibration. Conformal coating is available.

Support logic in VHDL is provided for integration with FPGA carrier cards. Specific support for Innovative carrier cards includes integration with Framework Logic tools that support VHDL and Matlab developers. The Matlab BSP supports real-time hardware-in-the-loop development using the graphical block diagram Simulink environment with Xilinx System Generator for the FMC integrated with the FPGA carrier card.

Software tools for Innovative carrier cards include host development C++ libraries and drivers for Windows and Linux, 32/64-bit including RTOS variants. Application examples demonstrating the module features are provided.

FMC-500M

* Sampling rates in an application depend on carrier and system design

This electronics assembly can be damaged by ESD. Innovative Integration recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

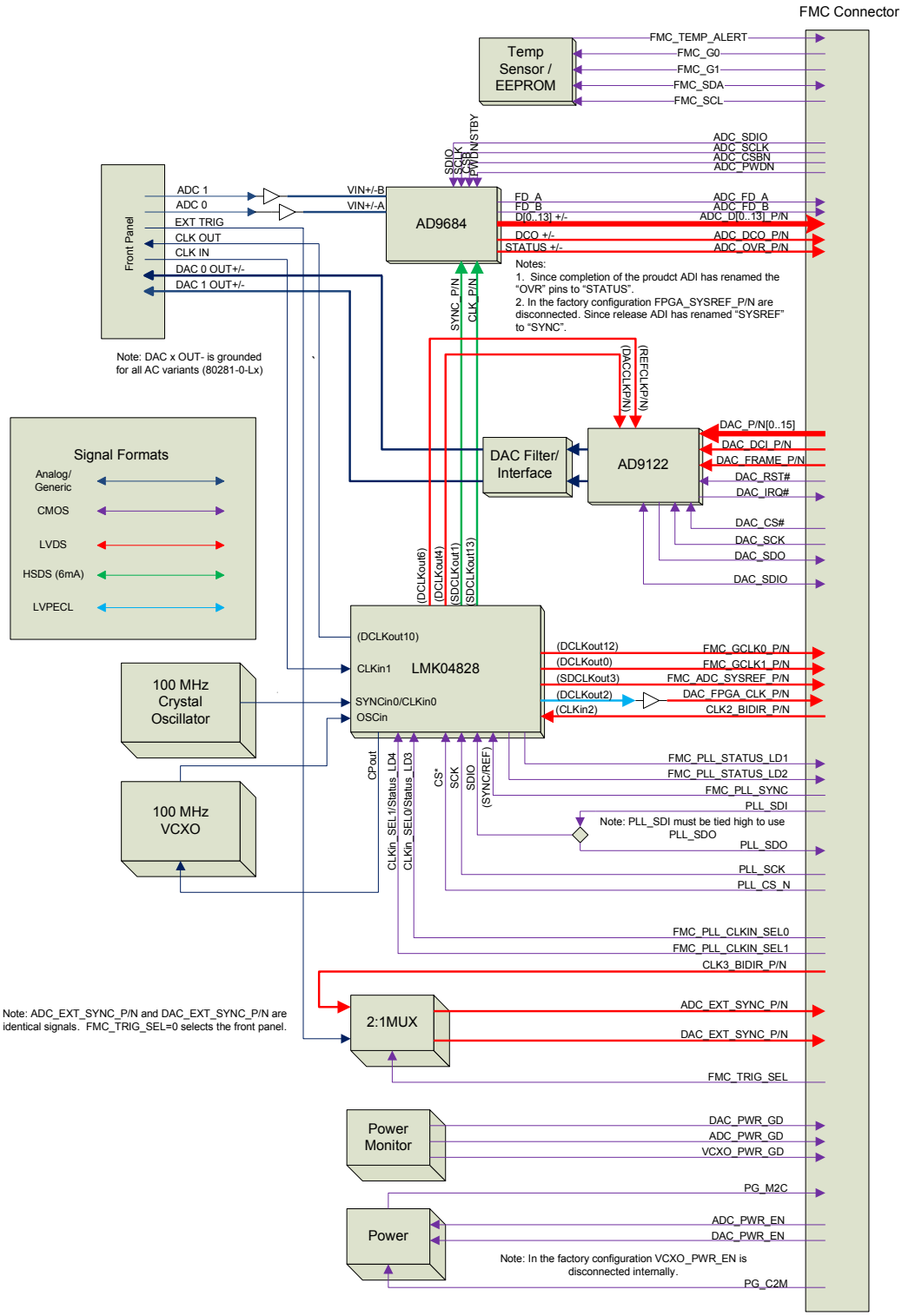
ORDERING INFORMATION

Product	Part No.	Description
FMC-500M	80281-<CFG>-<ER>	FMC module with dual 14-bit A/Ds (500 MSPS per channel), dual 16-bit DACs (1200 MSPS total update rate / 615 MSPS per channel), PLL and timing controls <CFG> is configuration. 0: AC-coupled analog ADC inputs and DAC outputs 2: DC-coupled analog ADC inputs and DAC outputs <ER> is environmental rating L0...L4.
Cables		
SSMC to BNC cable	67156	IO cable with SSMC (male) to BNC (male), 1 meter
Carrier Cards		
VPX6-COP	80262	3U VPX FPGA co-processor card with FMC site
PEX6-COP	80284	Desktop/server PCI Express FPGA co-processor card with FMC site
Embedded Computer Hosts		
ePC-K7	90502	Embedded PC with support for one FMC module; COM Express Type 6 i7 CPU; RF expansion tray; Windows, Linux
Mini-K7	90600	Miniature embedded PC with support for one FMC module; COM Express Type 6 Atom CPU; RF expansion tray; LCD display; Windows, Linux

<ER> corresponds to the Environmental Rating, L0...L4.

Physicals	
Form Factor	FMC VITA 57.1 single-width
Size	76.5 x 69 mm 10 mm mounting height
Weight	180g (approximate, contact factory if critical to application)
Hazardous Materials	Lead-free and RoHS compliant

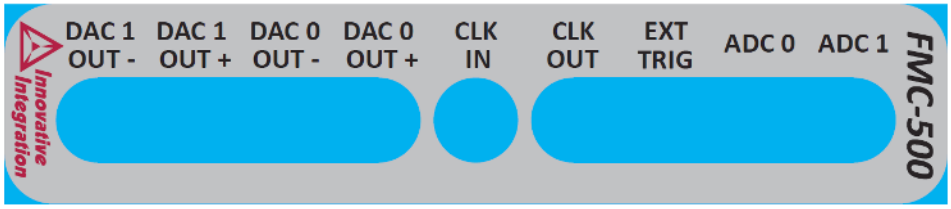
FMC-500M


FMC Connector
Temp Sensor / EEPROM
FMC_TEMP_ALERT
FMC_G0
FMC_G1
FMC_SDA
FMC_SCL
ADC_SDIO
ADC_SCLK
ADC_CSBN
ADC_PWDN
SDIO
SCLK
CSB
PWDN/STBY
Front Panel
ADC 1
ADC 0
EXT TRIG
CLK OUT
CLK IN
DAC 0 OUT+/-
DAC 1 OUT+/-
VIN+/-B
VIN+/-A
AD9684
FD_A
FD_B
D[0..13] +/-
DCO +/-
STATUS +/-
ADC_FD_A
ADC_FD_B
ADC_D[0..13]_P/N
ADC_DCO_P/N
ADC_OVR_P/N
Notes:
1. Since completion of the proudct ADI has renamed the "OVR" pins to "STATUS".
2. In the factory configuration FPGA_SYSREF_P/N are disconnected. Since release ADI has renamed "SYSREF" to "SYNC".
SYNC_P/N
CLK_P/N
Note: DAC x OUT- is grounded for all AC variants (80281-0-Lx)
(DACCLKP/N)
(REFCLKP/N)
Signal Formats
Analog/ Generic
CMOS
LVDS
HSDS (6mA)
LVPECL
DAC Filter/ Interface
AD9122
DAC_P/N[0..15]
DAC_DCI_P/N
DAC_FRAME_P/N
DAC_RST#
DAC_IRQ#
DAC_CS#
DAC_SCK
DAC_SDO
DAC_SDIO
(DCLKout6)
(DCLKout4)
SDCLKout1)
SDCLKout13)
(DCLKout10)
CLKin1
LMK04828
SYNCin0/CLKin0
OSCin
(DCLKout12)
(DCLKout0)
(SDCLKout3)
(DCLKout2)
(CLKin2)
FMC_GCLK0_P/N
FMC_GCLK1_P/N
FMC_ADC_SYSREF_P/N
DAC_FPGA_CLK_P/N
CLK2_BIDIR_P/N
100 MHz Crystal Oscillator
100 MHz VCXO
CPout
CLKin_SEL1/Status_LD4
CLKin_SEL0/Status_LD3
CS*
SCK
SDIO
(SYNC/REF)
FMC_PLL_STATUS_LD1
FMC_PLL_STATUS_LD2
FMC_PLL_SYNC
PLL_SDI
Note: PLL_SDI must be tied high to use PLL_SDO
PLL_SDO
PLL_SCK
PLL_CS_N
FMC_PLL_CLKIN_SEL0
FMC_PLL_CLKIN_SEL1
CLK3_BIDIR_P/N
Note: ADC_EXT_SYNC_P/N and DAC_EXT_SYNC_P/N are identical signals. FMC_TRIG_SEL=0 selects the front panel.
2:1MUX
ADC_EXT_SYNC_P/N
DAC_EXT_SYNC_P/N
FMC_TRIG_SEL
Power Monitor
DAC_PWR_GD
ADC_PWR_GD
VCXO_PWR_GD
PG_M2C
Power
ADC_PWR_EN
DAC_PWR_EN
Note: In the factory configuration VCXO_PWR_EN is disconnected internally.
PG_C2M

FMC-500M

Front Panel (Bezel) Detail

Front Panel Label	Schematic reference	Description
ADC 0	J1	ADC 0 Input. DC-coupled versions (-2-Lx) Load Impedance: 50 ohm termination to ground. Expected signal: 0 ± 1V (nominal) AC-coupled versions (-0-Lx) Load Impedance: 50 ohm AC termination to ground (DC open) Expected signal: Vdc ± 1V (nominal) (10 dBm), |Vdc| ≤ 5 V
ADC 1	J2	ADC 1 Input. (same terminations and input requirements as ADC 0)
EXT TRIG	J11	External Trigger Input. 50 DC termination to ground. Expected signal: 1.2V nominal threshold, 0 – 3.3V nominal limits.
CLK OUT	J12	Clock Output. AC-coupled, compatible with 50 ohm terminated load. Nominal signal output: 0.4 – 1.65 Vpp (hardware reconfigurable)
CLK IN	J13	External Clock Input. (When selected, used in place of internal 100 MHz reference clock.) Load Impedance: 50 ohms AC termination to ground (DC open). Expected signal: 0.3 – 3.3 Vpp, AC coupled
DAC 0 Out +	J6	DAC 0 Output (positive sense) DC-coupled versions (-2-Lx) Source Impedance: 50 ohms Nominal signal output: 0 ± 0.5V (into a 50 termination to ground.) AC-coupled versions (-0-Lx) Source Impedance: Approximately 150 ohms AC (DC short) Nominal signal output: 0 ± 0.5V (into a 50 ohm AC termination.)
DAC 0 Out -	J7	DAC 0 Output (negative sense) DC-coupled versions (-2-Lx) (same characteristics as DAC 0 Out +, except for polarity inversion) AC-coupled versions (-0-Lx) (In the AC coupled versions this output is grounded).
DAC 1 Out +	J8	DAC 1 Output (positive sense) (same characteristics as DAC 0 Out +)
DAC 1 Out -	J9	DAC 1 Output (negative sense) DC-coupled versions (-2-Lx) (same characteristics as DAC 1 Out +, except for polarity inversion) AC-coupled versions (-0-Lx) (In the AC coupled versions this output is grounded).



Note: 2.5 V logic inputs absolute maximum 2.8V, absolute minimum -0.3V

FMC-500M

Operating Environment Ratings

Modules rated for operating environment temperature, shock and vibration are offered. The modules are qualified for wide temperature, vibration and shock to suit a variety of applications in each of the environmental ratings L0 through L4 and 100% tested for compliance.

Environment Rating <ER>		**L0**	**L1**	**L2**	**L3**	**L4**
Environment		Office, controlled lab	Outdoor, stationary	Industrial	Vehicles	Military and heavy industry
Applications		Lab instruments, research	Outdoor monitoring and controls	Industrial applications with moderate vibration	Manned vehicles	Unmanned vehicles, missiles, oil and gas exploration
Cooling		Forced Air 2 CFM	Forced Air 2 CFM	Conduction	Conduction	Conduction
Operating Temperature		0 to +50C	-40 to +85C	-20 to +65C	-40 to +70C	-40 to +85C
Storage Temperature		-20 to +90C	-40 to +100C	-40 to +100C	-40 to +100C	-50 to +100C
Vibration	Sine	-	-	2g 20-500 Hz	5g 20-2000 Hz	10g 20-2000 Hz
	Random	-	-	0.04 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz	0.1 g^2/Hz 20-2000 Hz
Shock		-	-	20g, 11 ms	30g, 11 ms	40g, 11 ms
Humidity		0 to 95%, non-condensing	0 to 100%	0 to 100%	0 to 100%	0 to 100%
Conformal coating			Conformal coating	Conformal coating, extended temperature range devices	Conformal coating, extended temperature range devices, Thermal conduction assembly	Conformal coating, extended temperature range devices, Thermal conduction assembly, Epoxy bonding for devices
Testing		Functional, Temperature cycling	Functional, Temperature cycling, Wide temperature testing	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Temperature cycling, Wide temperature testing Vibration, Shock	Functional, Testing per MIL-STD-810G for vibration, shock, temperature, humidity

Minimum lot sizes and NRE charges may apply. Contact sales support for pricing and availability.

FMC-500M

Standard Features

Analog Inputs	
Inputs	2
Input Type	Single ended; AC or DC coupled
Nominal Input Impedance	50 ohm
A/D Device	Analog Devices AD9684 (500MSPS, 14-bit)
Resolution	14-bit
ADC Sample Rate	50 MHz to 500 MHz
Input Bandwidth	500 MHz (-3dB, est.) (AC-Coupled) 800 MHz (-3dB, est.) (DC-Coupled)

Analog Outputs	
Outputs	2
Output Range	+/-1.0V AC or DC-coupled into 50 ohm load.
Output Type	Single ended, AC or DC coupled
Output Impedance	DC coupled versions: 50 ohms AC coupled versions: Approx 150 ohms (DC short)
DAC Device	Analog Devices AD9122BCPZ
DAC Resolution	16-bit
DAC Update Rate	10 MHz to 1200 MHz

*Possible clock and sample rates in an application can depend on hardware configuration, carrier and system design

Clocks and Triggering	
Clock Sources	External, or Internal, based on Texas Instruments LMK04828B. VCO0: 2370 – 2630 MHz VCO1: 2920 – 3080 MHz Est. jitter for 1.25 GHz clock output: < 135 fs (10kHz – 20 MHz) < 150 fs (100 Hz – 150 MHz) (based on 2.5 GHz VCO using ÷ 2 output divider)
PLL Reference	External or 100 MHz on-card 100 MHz ref is ±50 ppm 0 to +70C
PLL Resolution	≥ 4.77 kHz using external reference (Assumes PLL is configured with 16,383 divider ratio. Requires adjustment of on-board PLL filter and parameters.) ≤ 1 MHz using internal reference. (Note that this refers to VCO resolution. See "PLL Notes" below for further details.)
Phase Noise	-130 dBc / Hz @ 100 kHz offset (measured at reference frequency)
Triggering	External, software, acquire N frame Decimation 1:1 to 1:4095 in FPGA Channel Clocking All channels are synchronous Multi-card Synchronization External triggering input is used to synchronize sample clocks or an external clock and trigger may be used.

Analog Channels Crosstalk	Adjacent Channel	< -70	dB	Measured on terminated victim channel, other 95% FS 70.1 MHz sine
	A/D to/from D/A	< -90	dB	Measured on terminated victim channel, other 95% FS 70.1 MHz sine

FMC Interface	
IO	LA[33:0] pairs, HA[22:0] pairs, HB[12:0] pairs
IO Standards	FMC compliant. Differential (LVDS) or LVCMOS (1.7 – 3.3V) Refer to block diagram (p.3) and Pin Assignment (pp. 12 – 16) for details.
Required voltages	3.3V, 12V VADJ = 1.7 to 3.3 V

*Possible rates in an application can depend on hardware configuration, carrier and system design

Power		
All AC coupled	Total	9.52W (12.16W if external Vadj current is included)
	3.3 V	846.1 mA (2.79 W)
	12 V	560.3 mA (6.73 W)
	2.5V Vadj	< 1.2 A (2.64 W)
All DC coupled	Total	11.61W (14.25W if external Vadj current is included)
	3.3V	846.1 mA (2.79 W)
	12V	734.5 mA (8.82 W)
	2.5V Vadj	< 1.2A (2.64 W)
Heat Sinking		Conduction cooling supported, system level thermal design may be required

FMC-500M

A/D ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter		Typ	Units	Notes
A/D Channels				
Bandwidth		800	MHz	-3dB, DC coupled inputs
		500	MHz	-3dB, AC coupled inputs
Flatness		+/-0.4	dB	50 to 500 MHz, AC Coupled
		+/-0.5	dB	0 to 500 MHz, DC Coupled
Range	AC Coupled	2	Vpp	Nominal
		10	dBm	Nominal in a 50 Ohm system
		2.6	Vpp	Absolute maximumz
		+/-10	V	DC withstanding from 0V
	DC Coupled	+/-0.42	V	Nominal from 0V
		2.5	dBm	Nominal in a 50 Ohm system
		+/-1	V	Absolute maximum from 0V
SNR		67.8, 62.3	dB	Fin = 10 MHz, 95% FS, sine sampled at 500 MSPS; AC,DC Coupled
		65.0, 61.6	dB	Fin = 170 MHz, 95% FS, sine sampled at 500 MSPS; AC,DC Coupled
		56.4, 52.7	dB	Fin = 765 MHz, 95% FS, sine sampled at 500 MSPS; AC,DC Coupled
ENOB		10.9, 10.0	bits	Fin = 10 MHz, 95% FS, sine sampled at 500 MSPS; AC, DC Coupled
		10.3, 9.9	bits	Fin = 170 MHz, 95% FS, sine sampled at 500 MSPS; AC,DC Coupled
		9.0, 8.0	bits	Fin = 765 MHz, 95% FS, sine sampled at 500 MSPS; AC,DC Coupled
SFDR		81.7, 78.5	dB	Fin = 10 MHz, 95% FS, sine sampled at 500 MSPS; AC,DC Coupled
		75.5, 73.6	dB	Fin = 170 MHz, 95% FS, sine sampled at 500 MSPS; AC,DC Coupled
		65.5, 55.0	dB	Fin = 765 MHz, 95% FS, sine sampled at 500 MSPS; AC,DC Coupled
THD		-79.6, -78.0	dBc	Fin = 10 MHz, 95% FS, sine sampled at 500 MSPS; AC,DC Coupled
		-75.0, -73.0	dBc	Fin = 170 MHz, 95% FS, sine sampled at 500 MSPS; AC,DC Coupled
		-64.3, -51.0	dBc	Fin = 765 MHz, 95% FS, sine sampled at 500 MSPS; AC,DC Coupled
NSD		-153 dBFS / Hz		Fin = 30 MHz, sine sampled at 500 MSPS
Offset Error (absolute value maximum)		1	mV	Factory calibration, average of 64K samples after warmup.
Gain Error (absolute value maximum)		0.5	%	Factory calibration after warmup.

D/A ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.

Parameter	Typ	Units	Notes
DAC Channels			
Analog Output Range	1000	mVpp	Typical, AC Coupled
	1000	mVpp	Typical, DC Coupled
Analog Output Bandwidth	600	MHz	DC Coupled, no sinc compensation
	600	MHz	AC Coupled, no sinc compensation
Output Amplitude Variation	0.7	dB	0-100 MHz, DC Coupled, no sinc compensation
	0.8	dB	1-100 MHz, AC Coupled, no sinc compensation
SFDR	68	dB	20 MHz sine output, 1.2 dBm, DC coupled
	70	dB	20 MHz sine output, 1.2 dBm, AC coupled
S/N	59.7	dB	70.1 MHz sine output, -6 dBfs, AC coupled
	58	dB	70.1 MHz sine output, -6 dBfs, DC coupled
THD	-62	dB	70.1 MHz sine output, -6 dBfs, AC coupled
	-49	dB	70.1 MHz sine output, -6 dBfs, DC coupled
Intermodulation Distortion	<-75	dB	70+/-0.1 MHz, -6dBfs, AC Coupled
Channel Crosstalk	<-85	dB	Aggressor = 125.1 MHz, -3 dBfs adjacent channel
Noise floor	-100	dB	AC or DC output
Gain Error	<0.5	% of FS	Calibrated
Offset Error	<10	mV	Calibrated

Notes

Gain Definition

FMC-500 is specified and tested with a 50 Ohm source impedance (unless otherwise noted). The FMC-500 nominal gain is approximately 1X or 0dB when calibrated, the voltage at the FMC-500 input equals the digital reading output. The internal hardware (raw) gain of the FMC-500 may be different, for example when DC coupled the A/D IC sees about twice the voltage applied at the FMC-500 input.

Variations in source impedance change the system gain. The 50 Ohm terminations in a RF system are rarely physical resistors (they are the Thévenin equivalent of the circuit). At lower input frequencies 50 Ohm source terminations are not common but are needed for continuity with higher frequency 50 Ohm measurements. This source 50 Ohm series termination forms a voltage divider with the FMC-500 input impedance reducing the source voltage by approximately ½ at the FMC-500 input. Replacing it with a series 0 Ohm source resistance will change the system gain about 2X in Voltage or 6 dB.

Digital Calibration Note

The FMC-500 can be digitally calibrated for offset and gain. However if the signal is clipped (outside the A/D range) the information is lost, so the raw gain is typically designed for a signal level at the A/D that is slightly less than A/D Full Scale in the bandwidth of interest to allow the nominal input range to be measured accurately without clipping when digitally calibrated.

PLL Notes

The output clock is produced by an integer division (1 – 32) of the VCO output. The LMK048028 has two on-chip VCOs: one with a tuning range of 2370 – 2630 MHz and another with a tuning range of 2920 – 3080 MHz. These tuning ranges limit the range of frequencies that can be produced by integer division. For output clock frequencies below 263 MHz (2630 MHz / 10) some combination of VCO frequency and division ratio can be chosen to produce any arbitrary output clock frequency because the various divider output frequency ranges overlap (e.g., the VCO0 tuning range combined with a divide by 11 can produce 215.4545 – 239.0909 MHz while the same VCO divided by 10 can produce 237 – 263 MHz, which overlaps with the divide by 11 range). However, there are tuning range gaps above 263 MHz as shown in Table 1 on p. 11. For example, neither VCO can be divided by an integer to produce an output frequency of 390 MHz since it lies within the 385 – 395 MHz tuning gap. The closest frequency above is produced by VCO0 (2370 MHz / 6) and the closest frequency below is produced by VCO1 (3080 MHz / 8).

Beyond the ability to successfully synthesize a prescribed output clock frequency as outlined above, the tuning resolution limits the ability to realize the corresponding VCO output frequency exactly. The architecture of the loop requires that the VCO frequency be a rational fraction multiple (i.e., a quotient of integers) of the input reference frequency (in this case, 100 MHz). Two issues limit the achievable resolution: (1) the precision of the rational fraction necessary to produce the necessary VCO frequency and (2) the value of the feedback divide ratio (the numerator of the rational fraction) required to produce that VCO frequency since it affects the stability parameters of the PLL. The required divide ratios are not always obvious – for example, producing 81.6 MHz requires a VCO frequency of 2529.6 MHz (81.6 MHz x 31), which is (3162/125) x 100 MHz. However, producing 81.7 MHz requires a VCO frequency of 2532.7 MHz (81.7 MHz x 31) which is (25327 / 1000) x 100 MHz. For a loop that is nominally designed for a target divide ratio of 2500, this larger value of N (25327) would result in the loop going nearly unstable unless its component values are changed. To keep this loop stable we can compromise by allowing ourselves to produce a clock frequency that is close to, but not exactly equal to 81.7 MHz. For example, (1317/52) x 100 MHz would result in a VCO frequency of 2532.692308 MHz and a corresponding output clock frequency of 81.699752 MHz.

Outdiv	Fmin	Fmax	VCO0	VC01
10 - 32	74.0625	263	X	
Gap	263	263.3333		
9	263.3333	292.2222	X	
10	292	308		X
8	296.25	328.75	X	
9	324.4444	342.2222		X
7	338.5714	375.7143	X	
8	365	385		X
Gap	385	395		
6	395	438.3333	X	
7	417.1429	440		X
Gap	440	474		
5	474	526	X	
Gap	526	584		
5	584	616		X
4	592.5	657.5	X	
Gap	657.5	730		
4	730	770		X
Gap	770	790		
3	790	876.6667	X	
Gap	876.6667	973.3333		
3	973.3333	1026.667		X
Gap	1026.667	1185		
2	1185	1315	X	
Gap	1315	1460		
2	1460	1540		X

Table 1. Range of output clock frequencies showing gaps in the tuning range.

FMC-500M

FMC Connector Pin Assignments

P1 Pins	P1 Pin Name	FMC-500 Net
A1	GND	GND
A2	DP1_M2C_P	N/C
A3	DP1_M2C_N	N/C
A4	GND	GND
A5	GND	GND
A6	DP2_M2C_P	N/C
A7	DP2_M2C_N	N/C
A8	GND	GND
A9	GND	GND
A10	DP3_M2C_P	N/C
A11	DP3_M2C_N	N/C
A12	GND	GND
A13	GND	GND
A14	DP4_M2C_P	N/C
A15	DP4_M2C_N	N/C
A16	GND	GND
A17	GND	GND
A18	DP5_M2C_P	N/C
A19	DP5_M2C_N	N/C
A20	GND	GND
A21	GND	GND
A22	DP1_C2M_P	N/C
A23	DP1_C2M_N	N/C
A24	GND	GND
A25	GND	GND
A26	DP2_C2M_P	N/C
A27	DP2_C2M_N	N/C
A28	GND	GND
A29	GND	GND
A30	DP3_C2M_P	N/C
A31	DP3_C2M_N	N/C
A32	GND	GND
A33	GND	GND
A34	DP4_C2M_P	N/C
A35	DP4_C2M_N	N/C
A36	GND	GND
A37	GND	GND
A38	DP5_C2M_P	N/C
A39	DP5_C2M_N	N/C
A40	GND	GND

B1	CLK_DIR	3P3V
B2	GND	GND
B3	GND	GND
B4	DP9_M2C_P	N/C
B5	DP9_M2C_N	N/C
B6	GND	GND
B7	GND	GND
B8	DP8_M2C_P	N/C
B9	DP8_M2C_N	N/C
B10	GND	GND
B11	GND	GND
B12	DP7_M2C_P	N/C
B13	DP7_M2C_N	N/C
B14	GND	GND
B15	GND	GND
B16	DP6_M2C_P	N/C
B17	DP6_M2C_N	N/C
B18	GND	GND
B19	GND	GND
B20	GBTCLK1_M2C_P	N/C
B21	GBTCLK1_M2C_N	N/C
B22	GND	GND
B23	GND	GND
B24	DP9_C2M_P	N/C
B25	DP9_C2M_N	N/C
B26	GND	GND
B27	GND	GND
B28	DP8_C2M_P	N/C
B29	DP8_C2M_N	N/C
B30	GND	GND
B31	GND	GND
B32	DP7_C2M_P	N/C
B33	DP7_C2M_N	N/C
B34	GND	GND
B35	GND	GND
B36	DP6_C2M_P	N/C
B37	DP6_C2M_N	N/C
B38	GND	GND
B39	GND	GND
B40	RES0	N/C

FMC Connector Pin Assignments (cont.)

C1	GND	GND
C2	DP0_C2M_P	N/C
C3	DP0_C2M_N	N/C
C4	GND	GND
C5	GND	GND
C6	DP0_M2C_P	N/C
C7	DP0_M2C_N	N/C
C8	GND	GND
C9	GND	GND
C10	LA06_P	ADC_FD_B
C11	LA06_N	ADC_SDIO
C12	GND	GND
C13	GND	GND
C14	LA10_P	ADC_SCLK
C15	LA10_N	ADC_CSB_N
C16	GND	GND
C17	GND	GND
C18	LA14_P	ADC_OVR_P
C19	LA14_N	ADC_OVR_N
C20	GND	GND
C21	GND	GND
C22	LA18_P_CC	FMC_PLL_SYNC
C23	LA18_N_CC	ADC_FD_A
C24	GND	GND
C25	GND	GND
C26	LA27_P	VCXO_PWR_GD
C27	LA27_N	N/C
C28	GND	GND
C29	GND	GND
C30	SCL	FMC_SCL
C31	SDA	FMC_SDA
C32	GND	GND
C33	GND	GND
C34	GA0	FMC_G0
C35	12P0V	12P0V
C36	GND	GND
C37	12P0V	12P0V
C38	GND	GND
C39	3P3V	3P3V
C40	GND	GND

D1	PG_C2M	FMC_PG_C2M
D2	GND	GND
D3	GND	GND
D4	GBTCLK0_M2C_P	N/C
D5	GBTCLK0_M2C_N	N/C
D6	GND	GND
D7	GND	GND
D8	LA01_P_CC	ADC_D_P2
D9	LA01_N_CC	ADC_D_N2
D10	GND	GND
D11	LA05_P	ADC_D_P5
D12	LA05_N	ADC_D_N5
D13	GND	GND
D14	LA09_P	ADC_D_P7
D15	LA09_N	ADC_D_N7
D16	GND	GND
D17	LA13_P	ADC_D_P13
D18	LA13_N	ADC_D_N13
D19	GND	GND
D20	LA17_P_CC	FPGA_SYSREF_P
D21	LA17_N_CC	FPGA_SYSREF_N
D22	GND	GND
D23	LA23_P	N/C
D24	LA23_N	N/C
D25	GND	GND
D26	LA26_P	ADC_PWR_EN
D27	LA26_N	ADC_PWR_GD
D28	GND	GND
D29	TCK	N/C
D30	TDI	N/C
D31	TDO	N/C
D32	3P3VAUX	3P3V_AUX
D33	TMS	N/C
D34	TRST_L	N/C
D35	GA1	FMC_G1
D36	3P3V	3P3V
D37	GND	GND
D38	3P3V	3P3V
D39	GND	GND
D40	3P3V	3P3V

FMC Connector Pin Assignments (cont.)

E1	GND	GND
E2	HA01_P_CC	N/C
E3	HA01_N_CC	N/C
E4	GND	GND
E5	GND	GND
E6	HA05_P	N/C
E7	HA05_N	N/C
E8	GND	GND
E9	HA09_P	N/C
E10	HA09_N	N/C
E11	GND	GND
E12	HA13_P	N/C
E13	HA13_N	N/C
E14	GND	GND
E15	HA16_P	N/C
E16	HA16_N	N/C
E17	GND	GND
E18	HA20_P	N/C
E19	HA20_N	N/C
E20	GND	GND
E21	HB03_P	DAC_P15
E22	HB03_N	DAC_N15
E23	GND	GND
E24	HB05_P	DAC_P13
E25	HB05_N	DAC_N13
E26	GND	GND
E27	HB09_P	DAC_P10
E28	HB09_N	DAC_N10
E29	GND	GND
E30	HB13_P	DAC_P7
E31	HB13_N	DAC_N7
E32	GND	GND
E33	HB19_P	DAC_P1
E34	HB19_N	DAC_N1
E35	GND	GND
E36	HB21_P	DAC_P4
E37	HB21_N	DAC_N4
E38	GND	GND
E39	VADJ	VADJ
E40	GND	GND

F1	PG_M2C	PG_M2C
F2	GND	GND
F3	GND	GND
F4	HA00_P_CC	N/C
F5	HA00_N_CC	N/C
F6	GND	GND
F7	HA04_P	N/C
F8	HA04_N	N/C
F9	GND	GND
F10	HA08_P	N/C
F11	HA08_N	N/C
F12	GND	GND
F13	HA12_P	N/C
F14	HA12_N	N/C
F15	GND	GND
F16	HA15_P	N/C
F17	HA15_N	N/C
F18	GND	GND
F19	HA19_P	N/C
F20	HA19_N	N/C
F21	GND	GND
F22	HB02_P	DAC_EXT_SYNC_P
F23	HB02_N	DAC_EXT_SYNC_N
F24	GND	GND
F25	HB04_P	DAC_SCLK
F26	HB04_N	DAC_IRQ#
F27	GND	GND
F28	HB08_P	DAC_P9
F29	HB08_N	DAC_N9
F30	GND	GND
F31	HB12_P	DAC_FRAME_P
F32	HB12_N	DAC_FRAME_N
F33	GND	GND
F34	HB16_P	DAC_DCI_P
F35	HB16_N	DAC_DCI_N
F36	GND	GND
F37	HB20_P	DAC_SDO
F38	HB20_N	DAC_SDIO
F39	GND	GND
F40	VADJ	VADJ

FMC Connector Pin Assignments (cont.)

G1	GND	GND
G2	CLK1_M2C_P	FMC_GCLK1_P
G3	CLK1_M2C_N	FMC_GCLK1_N
G4	GND	GND
G5	GND	GND
G6	LA00_P_CC	ADC_DCO_P
G7	LA00_N_CC	ADC_DCO_N
G8	GND	GND
G9	LA03_P	ADC_D_P3
G10	LA03_N	ADC_D_N3
G11	GND	GND
G12	LA08_P	ADC_D_P6
G13	LA08_N	ADC_D_N6
G14	GND	GND
G15	LA12_P	ADC_D_P8
G16	LA12_N	ADC_D_N8
G17	GND	GND
G18	LA16_P	ADC_D_P10
G19	LA16_N	ADC_D_N10
G20	GND	GND
G21	LA20_P	ADC_D_P12
G22	LA20_N	ADC_D_N12
G23	GND	GND
G24	LA22_P	PLL_SDI
G25	LA22_N	PLL_SDO
G26	GND	GND
G27	LA25_P	ADC_PWDN
G28	LA25_N	FMC_TRIG_SEL
G29	GND	GND
G30	LA29_P	FMC_PLL_STATUS_LD1
G31	LA29_N	FMC_PLL_STATUS_LD2
G32	GND	GND
G33	LA31_P	FMC_PLL_CLKIN_SEL0
G34	LA31_N	FMC_PLL_CLKIN_SEL1
G35	GND	GND
G36	LA33_P	DAC_RST#
G37	LA33_N	DAC_CS#
G38	GND	GND
G39	VADJ	VADJ
G40	GND	GND

H1	VREF_A_M2C	N/C
H2	PRSNT_M2C_L	GND
H3	GND	GND
H4	CLK0_M2C_P	FMC_GCLK0_P
H5	CLK0_M2C_N	FMC_GCLK0_N
H6	GND	GND
H7	LA02_P	ADC_D_P1
H8	LA02_N	ADC_D_N1
H9	GND	GND
H10	LA04_P	ADC_D_P4
H11	LA04_N	ADC_D_N4
H12	GND	GND
H13	LA07_P	ADC_D_P0
H14	LA07_N	ADC_D_N0
H15	GND	GND
H16	LA11_P	ADC_D_P9
H17	LA11_N	ADC_D_N9
H18	GND	GND
H19	LA15_P	ADC_D_P11
H20	LA15_N	ADC_D_N11
H21	GND	GND
H22	LA19_P	FMC_ADC_SYSREF_P
H23	LA19_N	FMC_ADC_SYSREF_N
H24	GND	GND
H25	LA21_P	ADC_EXT_SYNC_P
H26	LA21_N	ADC_EXT_SYNC_N
H27	GND	GND
H28	LA24_P	PLL_RESET
H29	LA24_N	PLL_GPO
H30	GND	GND
H31	LA28_P	PLL_SCK
H32	LA28_N	PLL_CS_N
H33	GND	GND
H34	LA30_P	VCXO_PWR_EN
H35	LA30_N	FMC_TEMP_ALERT
H36	GND	GND
H37	LA32_P	DAC_PWR_EN
H38	LA32_N	DAC_PWR_GD
H39	GND	GND
H40	VADJ	VADJ

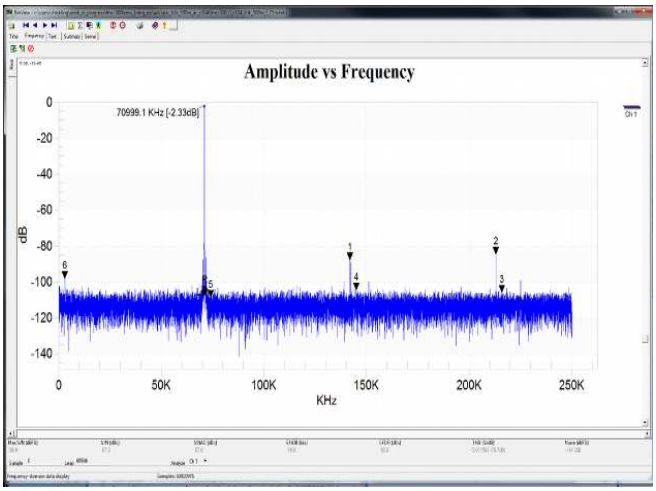
FMC Connector Pin Assignments (cont.)

J1	GND	GND
J2	CLK3_BIDIR_P	CLK3_BIDIR_P
J3	CLK3_BIDIR_N	CLK3_BIDIR_N
J4	GND	GND
J5	GND	GND
J6	HA03_P	N/C
J7	HA03_N	N/C
J8	GND	GND
J9	HA07_P	N/C
J10	HA07_N	N/C
J11	GND	GND
J12	HA11_P	N/C
J13	HA11_N	N/C
J14	GND	GND
J15	HA14_P	N/C
J16	HA14_N	N/C
J17	GND	GND
J18	HA18_P	N/C
J19	HA18_N	N/C
J20	GND	GND
J21	HA22_P	N/C
J22	HA22_N	N/C
J23	GND	GND
J24	HB01_P	DAC_P14
J25	HB01_N	DAC_N14
J26	GND	GND
J27	HB07_P	DAC_P11
J28	HB07_N	DAC_N11
J29	GND	GND
J30	HB11_P	DAC_P8
J31	HB11_N	DAC_N8
J32	GND	GND
J33	HB15_P	DAC_P3
J34	HB15_N	DAC_N3
J35	GND	GND
J36	HB18_P	DAC_P2
J37	HB18_N	DAC_N2
J38	GND	GND
J39	VIO_B_M2C	VADJ
J40	GND	GND

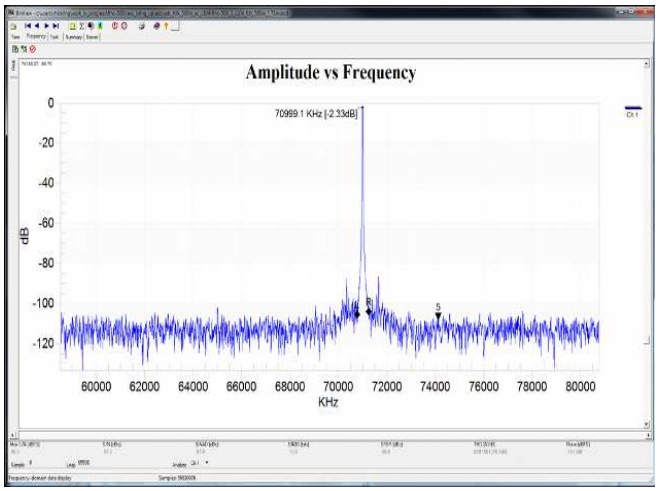
K1	VREF_B_M2C	N/C
K2	GND	GND
K3	GND	GND
K4	CLK2_BIDIR_P	CLK2_BIDIR_P
K5	CLK2_BIDIR_N	CLK2_BIDIR_N
K6	GND	GND
K7	HA02_P	N/C
K8	HA02_N	N/C
K9	GND	GND
K10	HA06_P	N/C
K11	HA06_N	N/C
K12	GND	GND
K13	HA10_P	N/C
K14	HA10_N	N/C
K15	GND	GND
K16	HA17_P_CC	N/C
K17	HA17_N_CC	N/C
K18	GND	GND
K19	HA21_P	N/C
K20	HA21_N	N/C
K21	GND	GND
K22	HA23_P	N/C
K23	HA23_N	N/C
K24	GND	GND
K25	HB00_P_CC	DAC_FPGA_CLK_P
K26	HB00_N_CC	DAC_FPGA_CLK_N
K27	GND	GND
K28	HB06_P_CC	DAC_P12
K29	HB06_N_CC	DAC_N12
K30	GND	GND
K31	HB10_P	DAC_P6
K32	HB10_N	DAC_N6
K33	GND	GND
K34	HB14_P	DAC_P5
K35	HB14_N	DAC_N5
K36	GND	GND
K37	HB17_P_CC	DAC_P0
K38	HB17_N_CC	DAC_N0
K39	GND	GND
K40	VIO_B_M2C	VADJ

FMC-500M

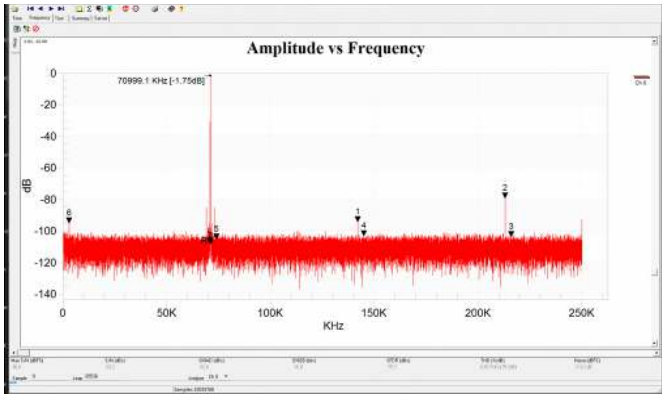
Representative ADC Performance



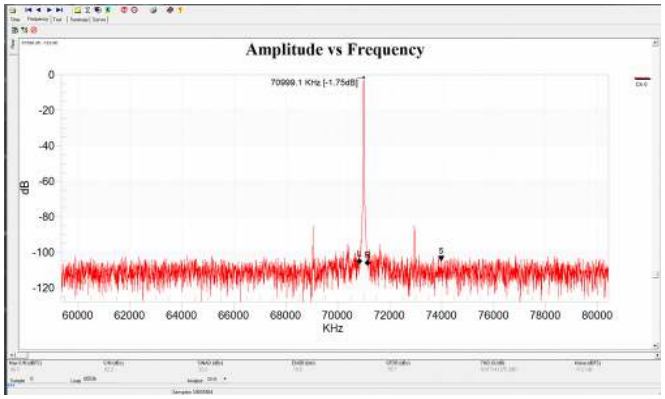
AC-Coupled A/D wideband signal quality, Fin = 71MHz, Fs = 500 MHz
Onboard PLL. Channel 1



AC-Coupled A/D narrowband signal quality, Fin = 71 MHz, Fs = 500 MHz
Onboard PLL. Channel 1

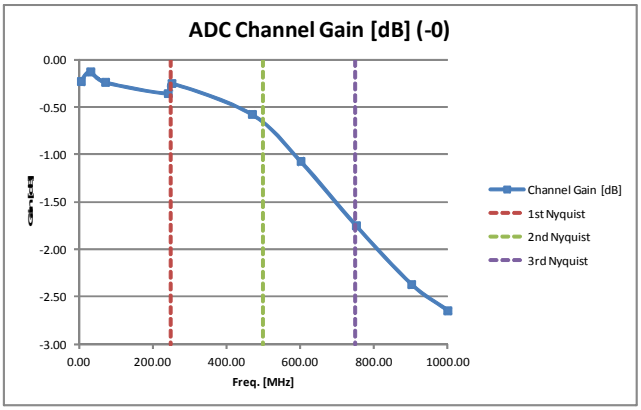


DC-Coupled A/D wideband signal quality, Fin = 71MHz, Fs = 500 MHz
Onboard PLL. Channel 0



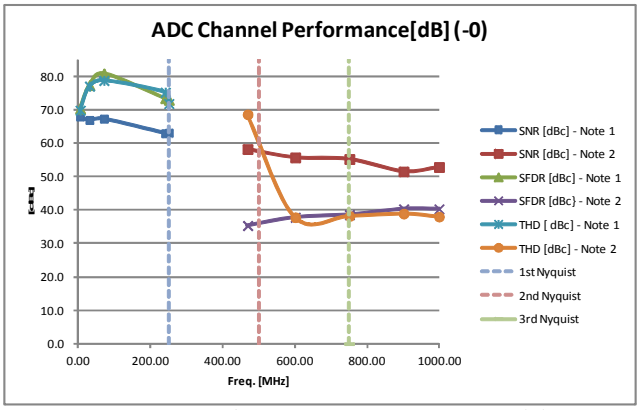
DC-Coupled A/D narrowband signal quality, Fin = 71 MHz, Fs = 500 MHz
Onboard PLL. Channel 0

FMC-500M



Frequency Response [dB] – AC coupled (Clock = 500 MHz)

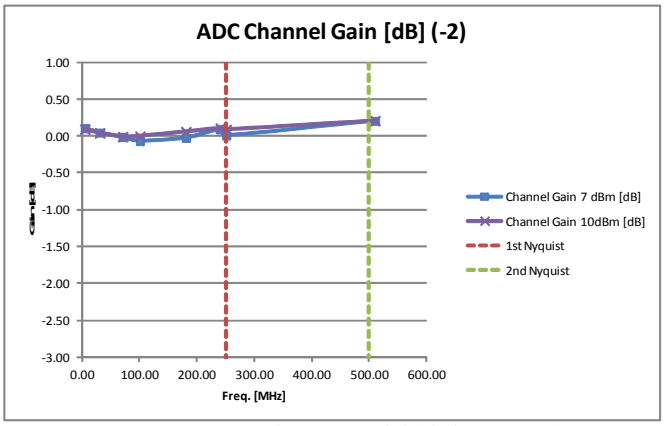
Note: 5 MHz data is provided for informational purposes only – it is outside the valid frequency range specified for the input transformer (> 30 MHz).



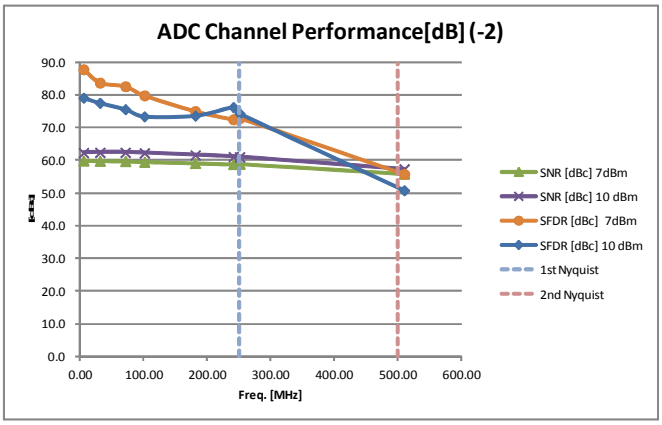
SNR & SFDR Performance versus Frequency – AC coupled

Note 1: Tested with bandpass filtering applied to signal source.

Note 2: Tested without filtering (noise partially reflects source signal quality).

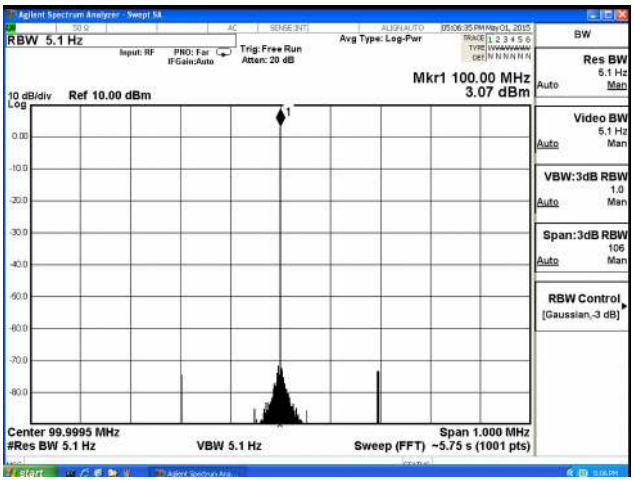


Frequency Response [dB] – DC coupled (Clock = 500 MHz)

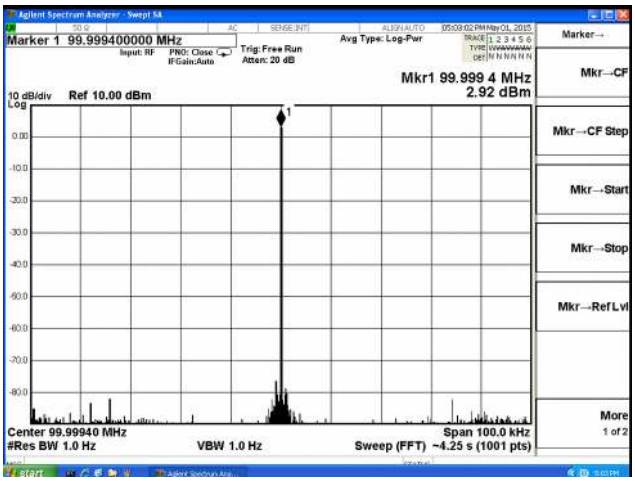


SNR & SFDR versus Frequency for 7 dBm and 10 dBm Input – DC coupled.

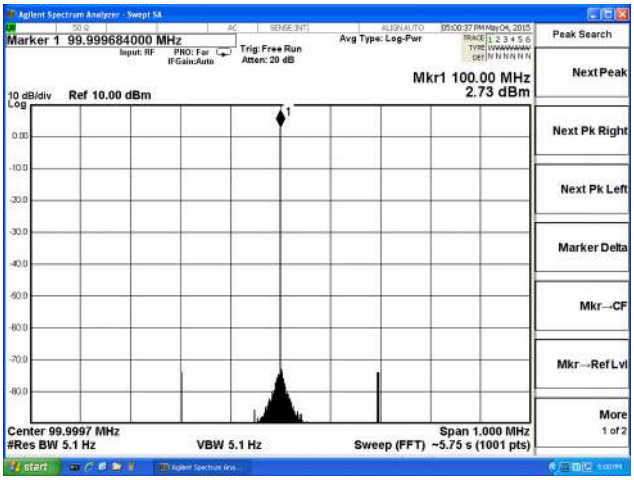
Representative DAC Performance



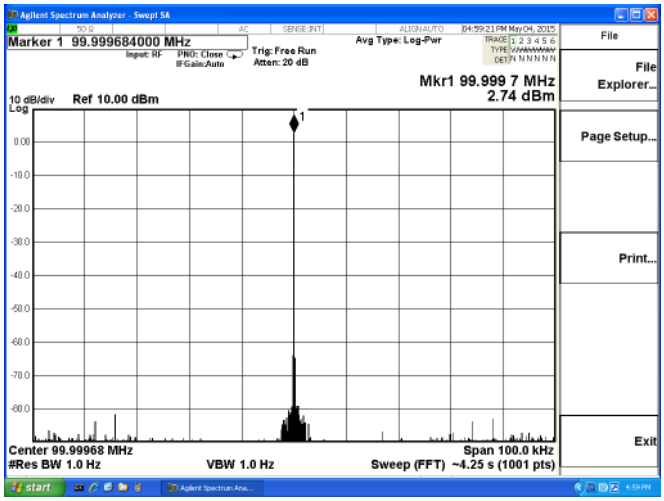
AC-Coupled Output Signal Quality
Fout = 100 MHz, Fs = 615 MHz.
(Resolution BW = 5.1 Hz)



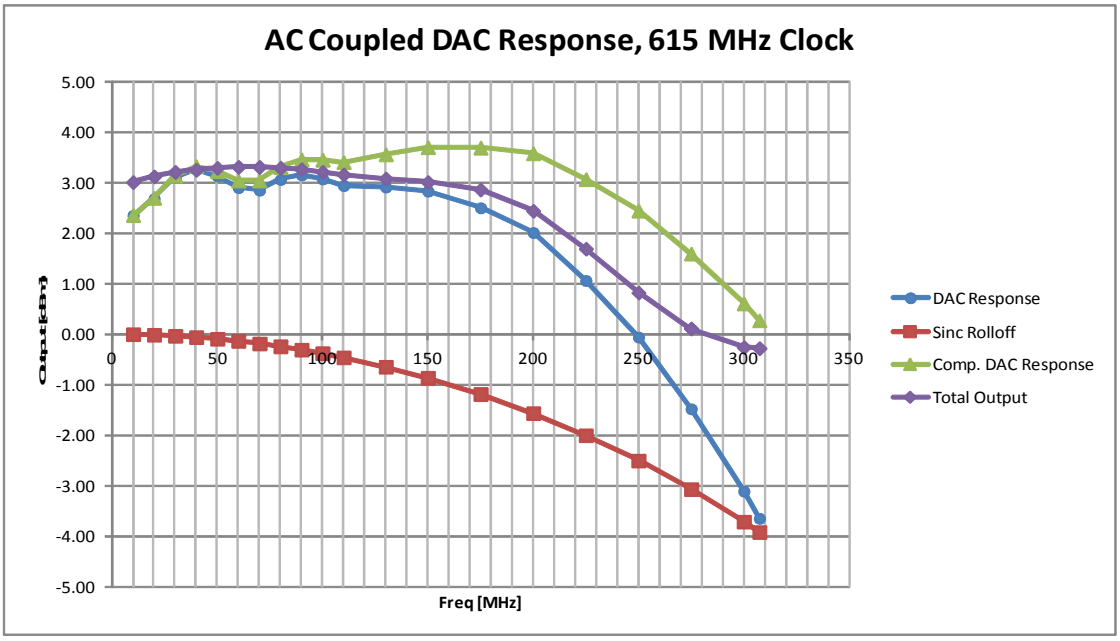
AC-Coupled Output Signal Quality
Fout = 100 MHz, Fs = 615 MHz.
(Resolution BW = 1 Hz)



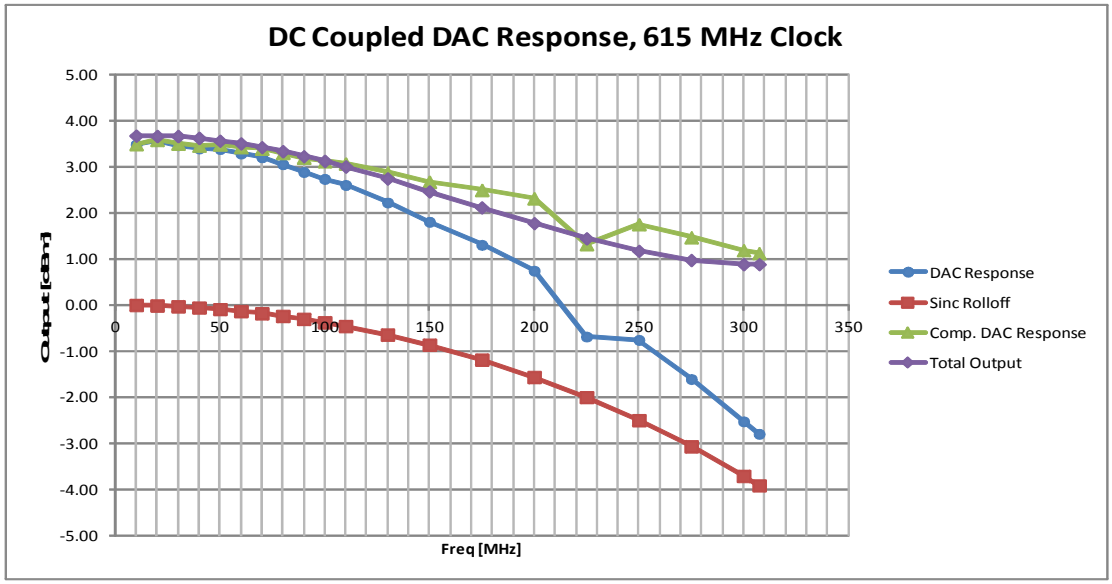
DC-Coupled Output Signal Quality
Fout = 100 MHz, Fs = 615 MHz.
(Resolution BW = 5.1 Hz)



DC-Coupled Output Signal Quality
Fout = 100 MHz, Fs = 615 MHz
(Resolution BW = 1 Hz)



AC-Coupled Output Frequency Response
Output level [dBm] of fundamental in blue, total power output in violet
For reference sinc rolloff is shown in red, and compensated output level in green.



DC-Coupled Output Frequency Response
Output level [dBm] of fundamental in blue, total power output in violet
For reference sinc rolloff is shown in red, and compensated output level in green.

FMC-500M

IMPORTANT NOTICES

Innovative Integration Incorporated reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to Innovative Integration's terms and conditions of sale supplied at the time of order acknowledgment.

Innovative Integration warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with Innovative Integration's standard warranty. Testing and other quality control techniques are used to the extent Innovative Integration deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

Innovative Integration assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using Innovative Integration products. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

Innovative Integration does not warrant or represent that any license, either express or implied, is granted under any Innovative Integration patent right, copyright, mask work right, or other Innovative Integration intellectual property right relating to any combination, machine, or process in which Innovative Integration products or services are used. Information published by Innovative Integration regarding third-party products or services does not constitute a license from Innovative Integration to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from Innovative Integration under the patents or other intellectual property of Innovative Integration.

Reproduction of information in Innovative Integration data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice.

Innovative Integration is not responsible or liable for such altered documentation. Resale of Innovative Integration products or services with statements different from or beyond the parameters stated by Innovative Integration for that product or service voids all express and any implied warranties for the associated Innovative Integration product or service and is an unfair and deceptive business practice. Innovative Integration is not responsible or liable for any such statements.

For further information on Innovative Integration products and support see our web site:

www.innovative-dsp.com

Mailing Address: Innovative Integration, Inc.

741 Flynn Road, Camarillo, California 93012