FMC-SDF

INTERCONNECT SYSTEMS
a molex company

FMC Module with four 24-bit, 625 kSPS A/D channels; two 18-bit D/A channels with on-board timing controls V1.1

FEATURES

- **Four A/D Input Channels**
  - ± 5V Input Range
  - 625 kSPS, 24-bit A/D
  - Differential Inputs
- **Two D/A Output Channels**
  - 2.1µs Settling Time, 18-bit D/A
  - ± 5V Output Range
- **Tachometer Input**
  - Schmitt-triggered for glitch tolerance
  - Can be configured to operate differentially
- **Sample Clocks and Timing Controls**
  - 10MHz, ±250 ppb stability on-board reference
  - Programmable PLL
  - Programmable Clock Frequency as low as 3.05 KHz
  - Integrated with FMC Triggers
- **FMC module, VITA 57.1**
  - High Pin Count no SERDES required
  - Compatible with 1.7 and 2.5V VADJ
  - Power Monitor and Controls
- 15W Typical Power Consumption
- Conduction Cooling per VITA 20 subset
- Environmental Ratings for -40 to 85C, 9g RMS sine, 0.1g^2/Hz random vibration

APPLICATIONS

- Seismic Data Acquisition
- Audio and Acoustic Testing
- ATE
- Other High SNR Data Acquisition

SOFTWARE

- Data Acquisition, Logging and Analysis applications provided
- Windows/Linux Drivers
- C++ Host Tools
- VHDL/MATLAB Logic Tools

XILINX

The FMC-SDF module features four simultaneously sampling ADCs and a dual output DAC. High resolution sigma-delta ADCs and high-resolution DACs support high dynamic range applications such as audio, ATE, and seismic data acquisition.

Clock and trigger controls include support for consistent servo loop timing, counted frames, software triggering and external triggering. The sample rate clock is either an external clock or on-board programmable PLL clock source.

The FMC-SDF power consumption is 15 W for typical operation. The module may be conduction cooled using VITA20 standard and a heat spreading plate. Ruggedization levels for wide-temperature operation are available from -40 to +85C operation and 0.1 g^2/Hz vibration. Conformal coating is also available.

Support logic in VHDL is provided for integration with FPGA carrier cards. Specific support for ISI Interconnect Systems carrier cards includes integration with Framework Logic tools that support VHDL.

Software tools for ISI Interconnect Systems carrier cards include host development C++ libraries and drivers for Windows and Linux, 32/64-bit including RTOS variants. Application examples demonstrating the module features are provided.
* Sampling rates in an application depend on carrier and system design.

FMC-SDF

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Interconnect Systems International, LLC standard warranty. Production processing does not necessarily include testing of all parameters.

This electronics assembly can be damaged by ESD. Interconnect Systems International, LLC recommends that all electronic assemblies and components circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

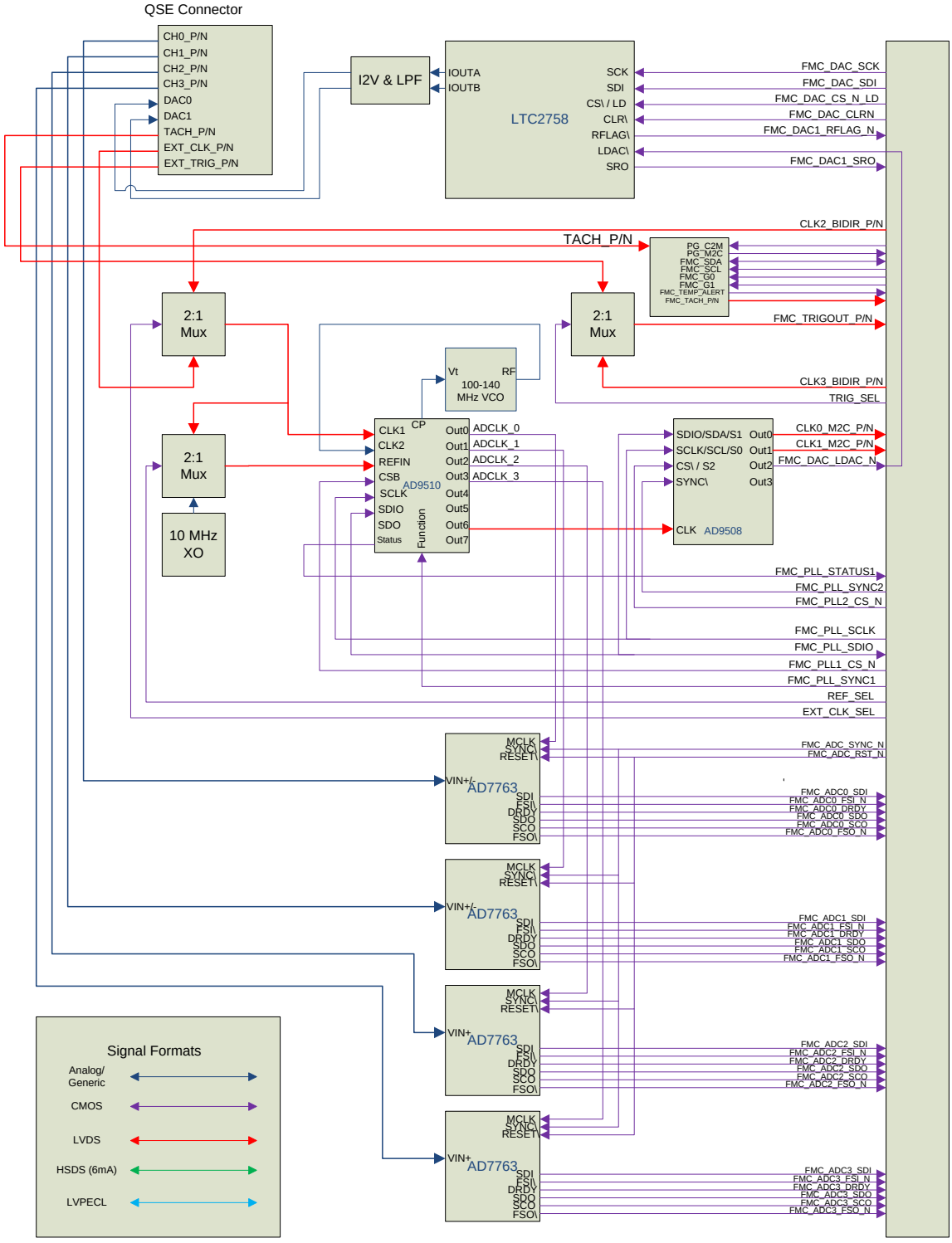
ORDERING INFORMATION

Product	Part Number	Description
FMC-SDF	80348-0-L0 Ruggedization	FMC module with four 24-bit A/Ds (625 kSPS per channel), two 18-bit DACs (2.1 µs settling time), on-board PLL. Ruggedization options may be available. Contact ISISales@molex.com .
Cables		
Ribbon Cable	67227	Ribbon Coaxial Cable connecting FMC module to breakout module
Breakout	80350-1-L0	Breakout module with all SMA connectors
FMC Hosts		
PEX-COP	80284-0-L0	PEX6-COP with LX240T-1 Speed FPGA, Gen2 x8 PCIe, x4 Aurora Port, 4 MB QDR, Dual Sample Clock Inputs
	80284-1-L0	PEX6-COP with LX240T-2 Speed FPGA, Gen2 x8 PCIe, x4 Aurora Port, 4 MB QDR, Dual Sample Clock Inputs
	80284-2-L0	PEX6-COP with LX315T-1 Speed FPGA, Gen2 x8 PCIe, x4 Aurora Port, 4 MB QDR, Dual Sample Clock Inputs
	80284-3-L0	PEX6-COP with LX315-2T-2 Speed FPGA, Gen2 x8 PCIe, x4 Aurora Port, 4 MB QDR, Dual Sample Clock Inputs
	80284-5-L0	PEX6-COP with LX550T-1 Speed FPGA, Gen2 x8 PCIe, x4 Aurora Port, 4 MB QDR, Dual Sample Clock Inputs
	80284-6-L0	PEX6-COP with SX475T-2 Speed FPGA, Gen2 x8 PCIe, x4 Aurora Port, 4 MB QDR, Dual Sample Clock Inputs
PEX7-COP	80382-0-L0	PEX7-COP with K325T-2 Speed FPGA, Gen2 x8 PCIe, x8 10.0 Gbps MGT lanes, External Clock and Trigger, Onboard USB JTAG Programmer
	80382-1-L0	PEX7-COP with K410T-2 Speed FPGA, Gen2 x8 PCIe, x8 10.0 Gbps MGT lanes, External Clock and Trigger, Onboard USB JTAG Programmer

Embedded Computers		
ePC-K7	90502-3-L0	ePC-K7 Instrument with Xilinx Kintex 7 K325T2 FPGA, EXPRESS-SL-I7-6820EQ 32 GB ECC ET, x2 1Gbe Ethernet, x2 USB 3.0 + x1 USB 2.0, x4 SATA III, IEEE-1588 or GPS optional, Clock and Trigger I/O, Conduction or Convection Cooled
	90502-4-L0	ePC-K7 Instrument with Xilinx Kintex 7 K410T-2 FPGA, EXPRESS-SL-I7-6820EQ 32 GB ECC ET, x2 1Gbe Ethernet, x2 USB 3.0 + x1 USB 2.0, x4 SATA III, IEEE-1588 or GPS optional, Clock and Trigger I/O, Conduction or Convection Cooled

BLOCK DIAGRAM

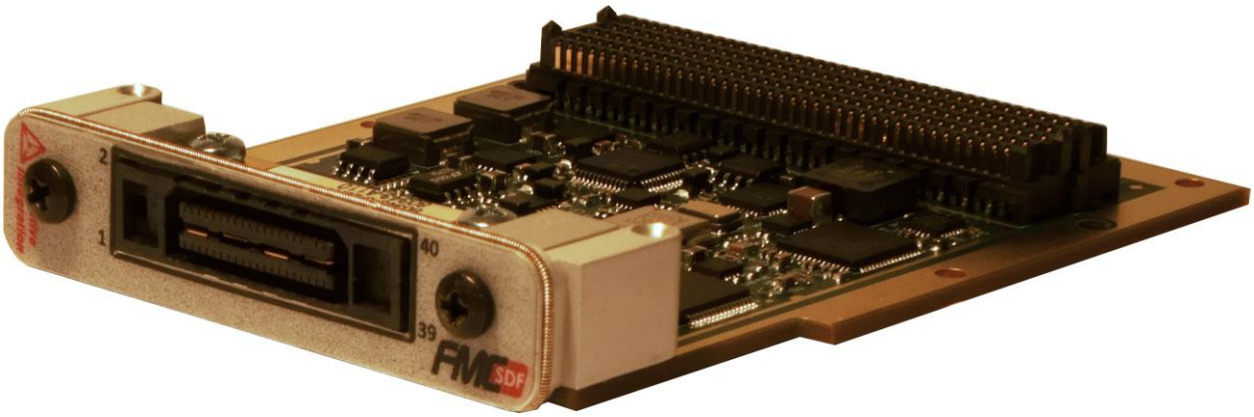
FMC-SDF Detailed Block Diagram



J2 (SAMTEC QSE-020-01-L-D-A) Connection Detail

Signal Name	J2 Pin Assignment	Description
CH0_P CH0_N CH1_P CH1_N CH2_P CH2_N CH3_P CH3_N	1 5 9 13 4 8 12 16	The four ADC channel inputs. Full-scale range is ±5V.
DAC0 DAC1	17 20	The two DAC channel outputs. Full-scale range is ±5V.
TACH_P TACH_N	21 24	The differential tachometer input. Using a hysteresis comparator (Schmitt trigger), the input is shipped with TACH_N connected to 2.5V, but can be modified such that TACH_P and TACH_N function differentially. Contact factory for detailed information.
EXT_TRIG_IN_P EXT_TRIG_IN_N	28 32	External Trigger Input. AC-coupled, differential termination 100 ohms. Nominally LVDS levels.
EXT_CLK_P EXT_CLK_N	25 29	External Clock Input. AC-coupled, differential termination 100 ohms. Nominally LVDS levels.

Note: 2.5 V logic inputs absolute maximum 2.8V, absolute minimum -0.3V



FMC-SDF

Standard Features

Analog Inputs	
Inputs	4
Input Ranges	± 5V
Input Type	Differential DC Coupled
Input Impedance	4 kΩ differential 2.5 kΩ single ended
A/D Device	Analog Devices AD7763
A/D Resolution	24-bit
A/D Sample Rate	Up to 625 kSPS ** Decimation feature in logic used for lower data rates
Data Format	2's complement, 24-bit integer
Connector	Samtec QSE-020-01-L-D-A
Calibration	Factory calibrated. Gain and offset errors are digitally corrected in the FPGA. Non-volatile EEPROM coefficient memory.

Analog Outputs	
Outputs	2
Output Ranges	± 5V
Output Type	Single ended DC Coupled
Output Impedance	50 Ω (Back-terminated to guard against overshoot/undershoot. DC load should be high impedance > 1kΩ.)
DAC Device	Linear Technology LTC2758
DAC Resolution	18-bit
DAC Update Rate	<= 400 kHz (if both channels are simultaneously updated. Will function faster if only one channel is used).
Connector	Samtec QSE-020-01-L-D-A

Clocks and Triggering	
Clock Sources	External, or Internal, based on Analog Devices AD9510 followed by AD9508. VCO: 110 – 150 MHz
Input Type	Single ended, AC coupled
Tachometer Input	Input threshold: 2.5 V Sensitivity/Hysteresis: ~100 mV
External Clock Input Range	TBD Vpp
External Trigger Input Range	TBD Vpp
Input Impedance	50 Ω

Clocks and Triggering	
Clock Sources	Internal, based on Analog Devices AD9510/AD9508 or External
PLL Output	VCO: 110 – 150 MHz AD9510: 3.4375 – 150 MHz AD9508: 3.3569 kHz – 150 MHz
PLL Jitter	Est. Jitter < 350 fs RMS
PLL Resolution	≥ 12 kHz using 10 MHz reference
Phase Noise	-155 dBc / Hz @ 100 kHz offset
PLL Programming	Via SPI through FMC connector
PLL Reference	External or 10 MHz on-card 10 MHz ref is ±250 ppb -40 to 85ºC
Triggering	External, software, acquire N frame
Decimation	1:1 to 1:4095 in FPGA
Channel Clocking	All channels are synchronous
Multi-card Synchronization	External triggering, clock, and PLL reference are supported.

Acquisition Monitoring	
Alerts	Trigger, Queue Overflow, Channel Over-range, Timestamp Rollover, Temperature Warning, Temperature Failure, PLL Unlocked

Power Management	
Alarms	Software programmable warning and failure levels
Over-temp Monitor	Disables analog IO power supplies
Power Control	Channel enables and power enables
Heat Sinking	Conduction cooling supported. System level thermal design may be required

FMC Interface	
IO	LA[33:0] pairs, HA[22:0] pairs, HB[12:0] pairs
IO Standards	LA: LVDS HA: LVDS HB: LVCMOS 1.7V to 3.3V
Required Voltages	3.3V, 12V VADJ = 1.7V to 3.3V

Physicals	
Form Factor	Single width FMC VITA 57.1
Size	76.5 x 69 mm
Weight	180g (approximate, contact factory if critical to application)
Hazardous Materials	Lead-free and RoHS compliant

ABSOLUTE MAXIMUM RATINGS

Exposure to conditions exceeding these ratings may cause damage!

Parameter	Min	Max	Units	Conditions
Supply Voltage, 3.3V to GND	3.1	+3.6	V	
Supply Voltage, VPWR to GND	4.5	14	V	
Operating Temperature	0	70	C	Non-condensing, conduction cooling
Storage Temperature	-40	100	C	
ESD Rating	-	2k	V	Human Body Model
Vibration	-	9	g	9-200 Hz, Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)
Shock	-	40	g peak	Class 3.3 per ETSI EN 300 019-1-3 V2.1.2 (2003-04)

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Typ	Max	Units
Supply Voltage	3.15	+3.3	+3.45	V
Supply Voltage, Nominal 12V VPWR	11.4	12	12.6	V, unless otherwise noted specified and tested with nominal 12V VPWR
Operating Temperature	0		50	C

	ELECTRICAL CHARACTERISTICS Over recommended operating free-air temperature range at 0°C to +60°C, unless otherwise noted.			
Group	**Parameter**	**Typ**	**Units**	**Notes**
Analog Inputs (Note 1)	Bandwidth	251	kHz	-0.1dB (Assumes default internal filter)
	SFDR	106.6 107.5 96.8 95.6 96.1 96.6	dBc	Fin = 1 kHz, ODR = 200 kHz, Vin = 1 Vpp Fin = 10 kHz, ODR = 200 kHz Vin = 1Vpp Fin = 1 kHz, ODR = 200 kHz, Vin = 5 Vpp Fin = 10 kHz, ODR = 200 kHz, Vin = 5 Vpp Fin = 1 kHz, ODR = 200 kHz, Vin = 10 Vpp Fin = 10 kHz, ODR = 200 kHz, Vin = 10 Vpp
	SNR	89.0 88.7 92.3 91.8 94.1 93.7	dBc	Fin = 1 kHz, ODR = 200 kHz, Vin = 1 Vpp Fin = 10 kHz, ODR = 200 kHz Vin = 1Vpp Fin = 1 kHz, ODR = 200 kHz, Vin = 5 Vpp Fin = 10 kHz, ODR = 200 kHz, Vin = 5 Vpp Fin = 1 kHz, ODR = 200 kHz, Vin = 10 Vpp Fin = 10 kHz, ODR = 200 kHz, Vin = 10 Vpp
	THD	-105.9 -107.5 -95.8 -95.6 -93.6 -94.1	dBc	Fin = 1 kHz, ODR = 200 kHz, Vin = 1 Vpp Fin = 10 kHz, ODR = 200 kHz Vin = 1Vpp Fin = 1 kHz, ODR = 200 kHz, Vin = 5 Vpp Fin = 10 kHz, ODR = 200 kHz, Vin = 5 Vpp Fin = 1 kHz, ODR = 200 kHz, Vin = 10 Vpp Fin = 10 kHz, ODR = 200 kHz, Vin = 10 Vpp
Analog Outputs (Notes 2, 3)	SFDR	92.2 85.3 74.5 75.8 85.3 68.3 81.5 67.6	dBc	Fin = 1.1 kHz, ODR = 50 kHz, Vin = 5 Vpp Fin = 10.1 kHz, ODR = 50 kHz Vin = 5Vpp Fin = 1.1 kHz, ODR = 400 kHz, Vin = 5 Vpp Fin = 10.1 kHz, ODR = 400 kHz Vin = 5Vpp Fin = 1.1 kHz, ODR = 50 kHz, Vin = 10 Vpp Fin = 10.1 kHz, ODR = 50 kHz Vin = 10 Vpp Fin = 1.1 kHz, ODR = 400 kHz, Vin = 10 Vpp Fin = 10.1 kHz, ODR = 400 kHz Vin = 10Vpp
	SNR	84.2 73.7 78.0 74.9	dBc	Fin = 1.1 kHz, ODR = 50 kHz, Vin = 10 Vpp Fin = 10.1 kHz, ODR = 50 kHz Vin = 10 Vpp Fin = 1.1 kHz, ODR = 400 kHz, Vin = 10 Vpp Fin = 10.1 kHz, ODR = 400 kHz Vin = 10Vpp
	THD	-91.8 -74.6 -84.5 -74.1 -83.1 -68.5 -81.2 -66.0	dBc	Fin = 1.1 kHz, ODR = 50 kHz, Vin = 5 Vpp Fin = 10.1 kHz, ODR = 50 kHz Vin = 5Vpp Fin = 1.1 kHz, ODR = 400 kHz, Vin = 5 Vpp Fin = 10.1 kHz, ODR = 400 kHz Vin = 5Vpp Fin = 1.1 kHz, ODR = 50 kHz, Vin = 10 Vpp Fin = 10.1 kHz, ODR = 50 kHz Vin = 10 Vpp Fin = 1.1 kHz, ODR = 400 kHz, Vin = 10 Vpp Fin = 10.1 kHz, ODR = 400 kHz Vin = 10Vpp
	Static (DC input) INL	< ±2	LSBs	
	Channel Crosstalk	< -110	dB	Measured by connecting DAC outputs to two ADC inputs, with one channel enabled and one disabled. Sample rate = 400 kHz, frequency = 10.1 kHz.
	Random Noise	-130.7	dBFS/Hz	Measured with DAC conveying zero output and feeding ADC at 400 kHz sample rate. A 64K FFT is applied to the result.
Power	Supply Current (3.3V)	< 5.1	mA	(< 17 mW)
	Supply Current (12V)	1250	mA	(15 W)
	Supply Current (2.5V VADJ)	< 5.1	mA	(< 13 mW)
	Power Dissipation	15.03	W	Total

Notes

1. The ADC measurements were taken with the inputs driven complementary using a Stanford Research DS360 Function Generator. When driven single-ended, the THD and SFDR are slightly degraded.
2. The outputs of the DACs were driven directly into two ADC inputs of the same unit. Accordingly, some of the distortion measured (particularly at full amplitude) will have contributions from both the DACs and ADCs.
3. Although, the data sheet for the LTC2758 quotes a 2.1 µs typical settling time, the timing as implemented in the software and firmware (using the "Stream" application example) has a settling time of approximately 6 µs. Accordingly, the best results will be obtained when the DAC update rate is slower than 100 kHz.

Digital Calibration Note

The FMC-SDF can be digitally calibrated for offset and gain. However, if the signal is clipped (outside the A/D range) the information is lost, so the raw gain is typically designed for a signal level at the A/D that is slightly less than A/D Full Scale in the bandwidth of interest to allow the nominal input range to be measured accurately without clipping when digitally calibrated.

PLL Notes

The serial clock for the ADCs (MCLK) is produced by an integer division (1~32) of the VCO output generated by the AD9510. The VCO has a tuning range of 110 – 150 MHz and the crystal reference frequency is 10 MHz. The AD7763 can function with an MCLK frequency as low as 1 MHz; however, since the maximum divide ratio for the AD9510 (32) results in a range of 3.44 – 4.68 MHz, 3.44 MHz is the lowest frequency at which the ADC can be clocked in the FMC-SDF.

The input word rate of the LTC2758 is also produced by dividing down the VCO. The required relationship between the ADC sample output rate (AD_OCLK) and the DAC input rate (LDAC):

AD_OCLK x N1 x Decimation Rate / (N2 x N3) = LDAC

where:
– N1 is divider ratio for the AD9510 that produces MCLK for the AD7763 from the VCO,
– N2 is the divider ratio for the AD9510 that produces the clock that feeds the AD9508 from the VCO,
– N3 is the divider ratio for the AD9508 that produces LDAC (and CLK1_M2C_P/N), and
– "Decimation Rate" is either 32, 64, 128, or 256 (as the AD7763 is programmed)

One useful simplification is to set either N2 or N3 equal to the decimation rate. This would then require that the ADC and DAC interface rates be related by a fraction that is rational (i.e., the ratio of whole numbers). The "Stream" program places some further restrictions on this relationship to simplify calculation of the divider ratios.

FMC Connector Pin Assignments

A1	GND	GND	B1	CLK_DIR	3P3V
A2	DP1_M2C_P	N/C	B2	GND	GND
A3	DP1_M2C_N	N/C	B3	GND	GND
A4	GND	GND	B4	DP9_M2C_P	N/C
A5	GND	GND	B5	DP9_M2C_N	N/C
A6	DP2_M2C_P	N/C	B6	GND	GND
A7	DP2_M2C_N	N/C	B7	GND	GND
A8	GND	GND	B8	DP8_M2C_P	N/C
A9	GND	GND	B9	DP8_M2C_N	N/C
A10	DP3_M2C_P	N/C	B10	GND	GND
A11	DP3_M2C_N	N/C	B11	GND	GND
A12	GND	GND	B12	DP7_M2C_P	N/C
A13	GND	GND	B13	DP7_M2C_N	N/C
A14	DP4_M2C_P	N/C	B14	GND	GND
A15	DP4_M2C_N	N/C	B15	GND	GND
A16	GND	GND	B16	DP6_M2C_P	N/C
A17	GND	GND	B17	DP6_M2C_N	N/C
A18	DP5_M2C_P	N/C	B18	GND	GND
A19	DP5_M2C_N	N/C	B19	GND	GND
A20	GND	GND	B20	GBTCLK1_M2C_P	N/C
A21	GND	GND	B21	GBTCLK1_M2C_N	N/C
A22	DP1_C2M_P	N/C	B22	GND	GND
A23	DP1_C2M_N	N/C	B23	GND	GND
A24	GND	GND	B24	DP9_C2M_P	N/C
A25	GND	GND	B25	DP9_C2M_N	N/C
A26	DP2_C2M_P	N/C	B26	GND	GND
A27	DP2_C2M_N	N/C	B27	GND	GND
A28	GND	GND	B28	DP8_C2M_P	N/C
A29	GND	GND	B29	DP8_C2M_N	N/C
A30	DP3_C2M_P	N/C	B30	GND	GND
A31	DP3_C2M_N	N/C	B31	GND	GND
A32	GND	GND	B32	DP7_C2M_P	N/C
A33	GND	GND	B33	DP7_C2M_N	N/C
A34	DP4_C2M_P	N/C	B34	GND	GND
A35	DP4_C2M_N	N/C	B35	GND	GND
A36	GND	GND	B36	DP6_C2M_P	N/C
A37	GND	GND	B37	DP6_C2M_N	N/C
A38	DP5_C2M_P	N/C	B38	GND	GND
A39	DP5_C2M_N	N/C	B39	GND	GND
A40	GND	GND	B40	RES0	N/C

FMC Connector Pin Assignments (cont.)

C1	GND	GND
C2	DP0_C2M_P	N/C
C3	DP0_C2M_N	N/C
C4	GND	GND
C5	GND	GND
C6	DP0_M2C_P	N/C
C7	DP0_M2C_N	N/C
C8	GND	GND
C9	GND	GND
C10	LA06_P	FMC_DAC_SCK
C11	LA06_N	FMC_DAC_SDI
C12	GND	GND
C13	GND	GND
C14	LA10_P	FMC_DAC_CSN_LD
C15	LA10_N	FMC_DAC_CLRN
C16	GND	GND
C17	GND	GND
C18	LA14_P	FMC_DAC1_SRO
C19	LA14_N	FMC_DAC1_RFLAGN
C20	GND	GND
C21	GND	GND
C22	LA18_P_CC	FMC_TACH_OUT_P
C23	LA18_N_CC	FMC_TACH_OUT_N
C24	GND	GND
C25	GND	GND
C26	LA27_P	FMC_DAC1_LDAC
C27	LA27_N	N/C
C28	GND	GND
C29	GND	GND
C30	SCL	FMC_SCL
C31	SDA	FMC_SDA
C32	GND	GND
C33	GND	GND
C34	GA0	FMC_G0
C35	12P0V	12P0V
C36	GND	GND
C37	12P0V	12P0V
C38	GND	GND
C39	3P3V	3P3V
C40	GND	GND

D1	PG_C2M	FMC_PG_C2M
D2	GND	GND
D3	GND	GND
D4	GBTCLK0_M2C_P	N/C
D5	GBTCLK0_M2C_N	N/C
D6	GND	GND
D7	GND	GND
D8	LA01_P_CC	N/C
D9	LA01_N_CC	N/C
D10	GND	GND
D11	LA05_P	N/C
D12	LA05_N	N/C
D13	GND	GND
D14	LA09_P	N/C
D15	LA09_N	N/C
D16	GND	GND
D17	LA13_P	N/C
D18	LA13_N	N/C
D19	GND	GND
D20	LA17_P_CC	N/C
D21	LA17_N_CC	N/C
D22	GND	GND
D23	LA23_P	N/C
D24	LA23_N	N/C
D25	GND	GND
D26	LA26_P	N/C
D27	LA26_N	N/C
D28	GND	GND
D29	TCK	N/C
D30	TDI	N/C
D31	TDO	N/C
D32	3P3VAUX	3P3V_AUX
D33	TMS	N/C
D34	TRST_L	N/C
D35	GA1	FMC_G1
D36	3P3V	3P3V
D37	GND	GND
D38	3P3V	3P3V
D39	GND	GND
D40	3P3V	3P3V

FMC Connector Pin Assignments (cont.)

E1	GND	GND	F1	PG_M2C	PG_M2C
E2	HA01_P_CC	N/C	F2	GND	GND
E3	HA01_N_CC	N/C	F3	GND	GND
E4	GND	GND	F4	HA00_P_CC	N/C
E5	GND	GND	F5	HA00_N_CC	N/C
E6	HA05_P	N/C	F6	GND	GND
E7	HA05_N	N/C	F7	HA04_P	N/C
E8	GND	GND	F8	HA04_N	N/C
E9	HA09_P	N/C	F9	GND	GND
E10	HA09_N	N/C	F10	HA08_P	N/C
E11	GND	GND	F11	HA08_N	N/C
E12	HA13_P	N/C	F12	GND	GND
E13	HA13_N	N/C	F13	HA12_P	N/C
E14	GND	GND	F14	HA12_N	N/C
E15	HA16_P	N/C	F15	GND	GND
E16	HA16_N	N/C	F16	HA15_P	N/C
E17	GND	GND	F17	HA15_N	N/C
E18	HA20_P	N/C	F18	GND	GND
E19	HA20_N	N/C	F19	HA19_P	N/C
E20	GND	GND	F20	HA19_N	N/C
E21	HB03_P	N/C	F21	GND	GND
E22	HB03_N	N/C	F22	HB02_P	N/C
E23	GND	GND	F23	HB02_N	N/C
E24	HB05_P	N/C	F24	GND	GND
E25	HB05_N	N/C	F25	HB04_P	N/C
E26	GND	GND	F26	HB04_N	N/C
E27	HB09_P	N/C	F27	GND	GND
E28	HB09_N	N/C	F28	HB08_P	N/C
E29	GND	GND	F29	HB08_N	N/C
E30	HB13_P	N/C	F30	GND	GND
E31	HB13_N	N/C	F31	HB12_P	N/C
E32	GND	GND	F32	HB12_N	N/C
E33	HB19_P	N/C	F33	GND	GND
E34	HB19_N	N/C	F34	HB16_P	N/C
E35	GND	GND	F35	HB16_N	N/C
E36	HB21_P	N/C	F36	GND	GND
E37	HB21_N	N/C	F37	HB20_P	N/C
E38	GND	GND	F38	HB20_N	N/C
E39	VADJ	VADJ	F39	GND	GND
E40	GND	GND	F40	VADJ	VADJ

FMC Connector Pin Assignments (cont.)

G1	GND	GND	H1	VREF_A_M2C	N/C
G2	CLK1_M2C_P	CLK1_M2C_P	H2	PRSNT_M2C_L	GND
G3	CLK1_M2C_N	CLK1_M2C_N	H3	GND	GND
G4	GND	GND	H4	CLK0_M2C_P	CLK0_M2C_P
G5	GND	GND	H5	CLK0_M2C_N	CLK0_M2C_N
G6	LA00_P_CC	FMC_ADC0_SDI	H6	GND	GND
G7	LA00_N_CC	FMC_ADC0_FSI_N	H7	LA02_P	FMC_ADC2_DRDY
G8	GND	GND	H8	LA02_N	FMC_ADC2_SDO
G9	LA03_P	FMC_ADC1_SDI	H9	GND	GND
G10	LA03_N	FMC_ADC1_FSI_N	H10	LA04_P	FMC_ADC2_SCO
G11	GND	GND	H11	LA04_N	FMC_ADC2_FSO_N
G12	LA08_P	FMC_ADC2_SDI	H12	GND	GND
G13	LA08_N	FMC_ADC2_FSI_N	H13	LA07_P	FMC_ADC3_DRDY
G14	GND	GND	H14	LA07_N	FMC_ADC3_SDO
G15	LA12_P	FMC_ADC3_SDI	H15	GND	GND
G16	LA12_N	FMC_ADC3_FSI_N	H16	LA11_P	FMC_ADC3_SCO
G17	GND	GND	H17	LA11_N	FMC_ADC3_FSO_N
G18	LA16_P	FMC_ADC0_DRDY	H18	GND	GND
G19	LA16_N	FMC_ADC0_SDO	H19	LA15_P	N/C
G20	GND	GND	H20	LA15_N	N/C
G21	LA20_P	FMC_ADC0_SCO	H21	GND	GND
G22	LA20_N	FMC_ADC0_FSO_N	H22	LA19_P	N/C
G23	GND	GND	H23	LA19_N	N/C
G24	LA22_P	FMC_ADC1_DRDY	H24	GND	GND
G25	LA22_N	FMC_ADC1_SDO	H25	LA21_P	FMC_ADC_RST_N
G26	GND	GND	H26	LA21_N	FMC_ADC_SYNC_N
G27	LA25_P	FMC_ADC1_SCO	H27	GND	GND
G28	LA25_N	FMC_ADC1_FSO_N	H28	LA24_P	FMC_PLL1_CS_N
G29	GND	GND	H29	LA24_N	FMC_PLL_SCLK
G30	LA29_P	FMC_PLL_SDIO	H30	GND	GND
G31	LA29_N	FMC_ADC2_SDO	H31	LA28_P	FMC_TRIGOUT_P
G32	GND	GND	H32	LA28_N	FMC_TRIGOUT_N
G33	LA31_P	FMC_PLL_STATUS1	H33	GND	GND
G34	LA31_N	FMC_PLL_SYNC1	H34	LA30_P	TRIG_SEL
G35	GND	GND	H35	LA30_N	EXT_CLK_SEL
G36	LA33_P	N/C	H36	GND	GND
G37	LA33_N	FMC_PLL_SYNC2	H37	LA32_P	REF_SEL
G38	GND	GND	H38	LA32_N	FMC_TEMP_ALERT
G39	VADJ	VADJ	H39	GND	GND
G40	GND	GND	H40	VADJ	VADJ

FMC Connector Pin Assignments (cont.)

J1	GND	GND	K1	VREF_B_M2C	N/C
J2	CLK3_BIDIR_P	CLK3_BIDIR_P	K2	GND	GND
J3	CLK3_BIDIR_N	CLK3_BIDIR_N	K3	GND	GND
J4	GND	GND	K4	CLK2_BIDIR_P	CLK2_BIDIR_P
J5	GND	GND	K5	CLK2_BIDIR_N	CLK2_BIDIR_N
J6	HA03_P	N/C	K6	GND	GND
J7	HA03_N	N/C	K7	HA02_P	N/C
J8	GND	GND	K8	HA02_N	N/C
J9	HA07_P	N/C	K9	GND	GND
J10	HA07_N	N/C	K10	HA06_P	N/C
J11	GND	GND	K11	HA06_N	N/C
J12	HA11_P	N/C	K12	GND	GND
J13	HA11_N	N/C	K13	HA10_P	N/C
J14	GND	GND	K14	HA10_N	N/C
J15	HA14_P	N/C	K15	GND	GND
J16	HA14_N	N/C	K16	HA17_P_CC	N/C
J17	GND	GND	K17	HA17_N_CC	N/C
J18	HA18_P	N/C	K18	GND	GND
J19	HA18_N	N/C	K19	HA21_P	N/C
J20	GND	GND	K20	HA21_N	N/C
J21	HA22_P	N/C	K21	GND	GND
J22	HA22_N	N/C	K22	HA23_P	N/C
J23	GND	GND	K23	HA23_N	N/C
J24	HB01_P	N/C	K24	GND	GND
J25	HB01_N	N/C	K25	HB00_P_CC	N/C
J26	GND	GND	K26	HB00_N_CC	N/C
J27	HB07_P	N/C	K27	GND	GND
J28	HB07_N	N/C	K28	HB06_P_CC	N/C
J29	GND	GND	K29	HB06_N_CC	N/C
J30	HB11_P	N/C	K30	GND	GND
J31	HB11_N	N/C	K31	HB10_P	N/C
J32	GND	GND	K32	HB10_N	N/C
J33	HB15_P	N/C	K33	GND	GND
J34	HB15_N	N/C	K34	HB14_P	N/C
J35	GND	GND	K35	HB14_N	N/C
J36	HB18_P	N/C	K36	GND	GND
J37	HB18_N	N/C	K37	HB17_P_CC	N/C
J38	GND	GND	K38	HB17_N_CC	N/C
J39	VIO_B_M2C	N/C	K39	GND	GND
J40	GND	GND	K40	VIO_B_M2C	VADJ

FMC-SDF

Architecture and Features

The FMC-SDF module has four analog inputs that are simultaneously sampling channels of 24-bit, 625 KSPS A/D input. The A/D inputs have an input bandwidth up to 251KHz. There are two simultaneous D/A channels of 18-bit 476 KSPS output. Additional digital IO control bits from the FPGA are provided for application control and signaling.

Controls for triggering and clocks allow precise control over the collection of data. Trigger modes include frames of programmable size, external and software. Multiple FMC-SDF cards can sample simultaneously using external trigger inputs with synchronized sample clocks. The sample clock can be external or generated from the on-card PLL. The PLL can either use the on-card 10 MHz reference, or can use an external reference. When an external reference is used, the sample clock is synchronous to the reference.

All FMC modules produce hardware alerts that can be exploited by firmware and software tools to produce an on-screen alert mechanism. See below for further details.

Maximum Data Rates

The maximum data rates supported by the module are limited by the host modules PCI-e speed and or memory bandwidth.

It is important to qualify systems for performance when high data rates are required.

Cables

The FMC-SDF module uses ribbon cable assemblies for the analog I/O. The mating cable should have a Samtec connector and high impedance characteristic for best signal quality.

FMC Breakout

An FMC Breakout Board with or without a cable is available to make the FMC-SDF IO signals available on an external PCBA. There are several versions available for multiple requirements.

80350-0-L0	FMC BREAKOUT NO SMA CONNECTORS
80350-1-L0	FMC BREAKOUT ALL SMA CONNECTORS WITH 3 FT EQCD RIBBON COAXIAL CABLE
80350-4-L0	FMC BREAKOUT NO SMA NO CABLE
80350-5-L0	FMC BREAKOUT ALL SMA NO CABLE

The Pin Mapping between the FMC-SDF IO connector and FMC Breakout is shown in the table below.

FMC-SDF J2	SIGNAL	FMC Breakout	SIGNAL	FMC-Breakout Jack
Pin 3	CH3_P	Pin 3	DIFF_A0_N	A0_N
Pin 5	CH3_N	Pin 5	DIFF_A1_P	A1_P
Pin 9	CH2_P	Pin 9	DIFF_A2_P	A2_P
Pin 11	CH2_N	Pin 11	DIFF_A2_N	A2_N
Pin 15	CH1_P	Pin 15	DIFF_A3_N	A3_N
Pin 17	CH1_N	Pin 17	DIFF_A4_P	A4_P
Pin 21	CH0_P	Pin 21	DIFF_A5_P	A5_P
Pin 23	CH0_N	Pin 23	DIFF_A5_N	A5_N
Pin 31	TACH_P	Pin 31	DIFF_A7_N	A7_N
Pin 33	TACH_N	Pin 33	DIFF_A8_P	A8_P
Pin 37	EXT_CLK_P	Pin 37	DIFF_A9_P	A9_P
Pin 39	EXT_CLK_N	Pin 39	DIFF_A9_N	A9_N
Pin 38	EXT_TRIG_IN_P	Pin 38	DIFF_B9_P	B9_P
Pin 40	EXT_TRIG_IN_N	Pin 40	DIFF_B9_N	B9_N
Pin 26	DAC0	Pin 26	DIFF_B6_P	B6_P
Pin 30	DAC1	Pin 30	DIFF_B7_P	B7_P

NOTE 1: All SMA cases are connected to a common ground on the FMC Breakout Board.

NOTE 2: Unused pins on FMC-SDF J2 are all connected to FMC-SDF ground (AGND), but unused pins on FMC Breakout SAMTEC connector are open.

NOTE 3: FMC Breakout Board SAMTEC connector pins 41, 42, 43, and 44 are connected to FMC Breakout ground (GND).

FMC-SDF

FMC Hosts

FMC modules can be used in standard desktop system or compact PCI/PXIe using a host card. The host cards are software transparent.

PEX-COP (80284)	**PEX7-COP (80382)**	**ePC-K7 (90502)**
x8 PCIe FMC host with Virtex-6 FPGA	x8 PCIe FMC host with Kintex 7 FPGA	Windows/Linux embedded PC 8x USB, GbE, cable PCIe, VGA High speed x8 interconnect between modules GPS disciplined, programmable sample clocks and triggers to FMCs 1500 MB/s, 4 TB datalogger 9-18V operation
		

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